Connecting Multiple Intersil Encoders

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Introduction

In some systems, more video outputs are needed than are provided by a single Intersil NTSC/PAL video encoder. By using multiple encoders in the same system, additional outputs are available. For example, using two encoders provides a system with three composite, one S-video (Y/C), and one component (RGB or YUV) outputs.

When multiple encoders are required in the same system, they may be connected in one of three ways. The simplest method is to slave both encoders to a timing master. When a timing master is not available, the encoders may be the master in one of two ways.

This Application Note describes the three methods which may be used for multiple Intersil encoders in one system. This Application Note applies to the following Intersil encoders: HMP8154, HMP8156A, HMP8170, HMP8171, HMP8172, HMP8173, HMP8190, and HMP8191. Please refer to each part's datasheet for more information.

I^2C Slave Addressing

The Intersil encoders accept a slave address select input, SA. When SA is low, the encoder responds to slave address 0x40. When it is high, the encoder answers at slave address 0x42. With two encoders in the system, each can have its own slave address. With its own address, each encoder may be programmed to operate differently from the other.

In most applications, the encoders' basic operating modes should be programmed with all the same register values. The basic modes which should be the same include the video timing standard, input format, aspect ratio, and input resolution (8154/56 only). For dual master mode, the start and end blanking values must also be the same.

The methods described in this Application Note use just two encoders with SA tied high for the first encoder and low for the second. The methods may be extended to include additional encoders in the system by using a unary select line for each encoder.

Validation

The connection methods for multiple encoders shown in this Application Note have been demonstrated using the Intersil designed HMPVIDEVAL/ISA and HMP8154 EVAL1 evaluation boards. The VidEval board is an ISA bus based PC add in card with an HMP8115 decoder and HMP8154 encoder. The Eval1 board is a daughter card for the VidEval board with the second encoder.

Also, all the methods shown in this Application Note use the 8 bit YCbCr input format. Other input formats may also be used but all formats were not tested with all three connection modes described. When using input formats which use the CLK input to qualify which edges of CLK2 register data, the input timing is slightly different. The output timing is the same. Again, refer to the device datasheets for more information.

Slave Mode

In slave mode, two or more encoders are connected in parallel and setup to operate in slave mode. The timing control signals are driven by a timing master elsewhere in the system. Slave mode connections are show in Figure 1.

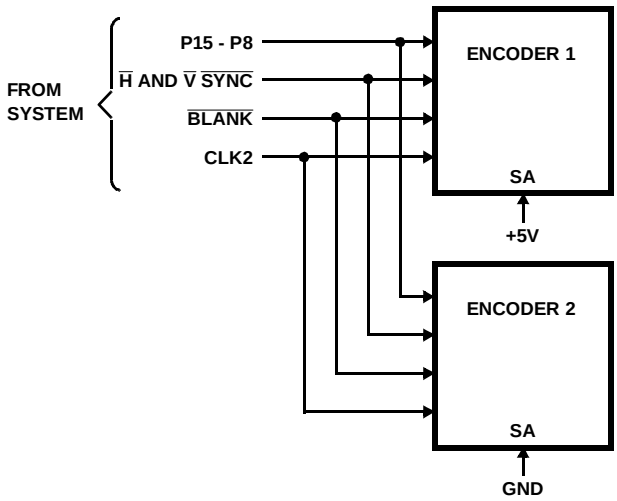

FIGURE 1. SLAVE MODE CONNECTIONS

Output Blanking

If the blanking signal is not available in the system, then each encoder should output its own $\overline{\text{BLANK}}$ signal. Since both encoders receive the same syncs and clocks, the blank signal from one encoder will be the same as the other. Since they are the same, either signal may be used as input to the system. When both encoders output $\overline{\text{BLANK}}$, the two signals should not be connected together.

BT.656

Figure 1 shows the syncs and blank as separate input signals. The encoders may also be slaved via BT.656 SAV and EAV codes embedded in the pixel data. When operating with the BT.656 input data format, the encoders output the H and V sync and blanking signals so they should not be connected together as shown in the figure.

Mixed Master Mode

In mixed master mode, the encoders generate all the syncs and blank signals to drive the rest of the system. To better match the timing delays of the encoders, one encoder generates the syncs for all of the system while the other generates the blanking signal.

There are two ways that mixed master mode may be implemented. In fast data mode, the encoders are connected directly together but the system supplying data to the encoders must provide data immediately after blank is asserted. In delayed data mode, a register delay is required from the first encoder to the second but the data may arrive a clock cycle after blank is asserted.

In both mixed master modes, the first encoder is programmed to input syncs and output blank. The second encoder is programmed to output syncs and input blank. The $\overline{\text{BLANK}}$ timing select bit in the timing I/O register at subaddress 4 sets the data mode.

Delayed Data Mode

The default value for the blank timing select bit is 0 and delayed data mode is selected. With the bit cleared, the encoder generating $\overline{\text{BLANK}}$ outputs it one clock cycle before requiring the pixel data. At the other encoder where blank is an input, the bit's value doesn't matter and the encoder always requires blank and the pixel data to arrive at the same time. The register delay of $\overline{\text{BLANK}}$ from the first encoder to the second adjusts the signal so that it arrives at the second encoder at the same time as the data.

The connections for delayed data mixed master mode are shown in Figure 2. Timing diagrams of the signals required for each implementation are also shown in the figure.

Fast Data Mode

When the blank timing select bit is set, fast data mode is selected. In fast data mode, the encoder generating $\overline{\text{BLANK}}$ outputs the signal at the same time that it requires the pixel data. At the other encoder where blank is an input, the bit's value doesn't matter and the encoder always requires blank and the pixel data to arrive at the same time. In a synchronous clocked system, the circuits supplying the data must have data ready for the encoders before $\overline{\text{BLANK}}$ is asserted.

The connections for fast data mixed master mode are shown in Figure 3. Timing diagrams of the signals required for each implementation are also shown in the figure.

Timing Issues

When mixed master mode is used, the output timing of the two encoders is not the same. The timing of each encoder's video output with respect to the system syncs and blank is shown in Figure 4. Note that Figure 4 is not drawn to scale. Also refer to Tech Brief TB368, "Understanding Video Timing with Digital Video Encoders," for more information about the encoder's timing.

As shown in Figure 4, the unblanked analog video data starts and ends at the same time for each encoder. However, the analog sync tips in the video from the first encoder occur about 0.34µs after those from the second encoder.

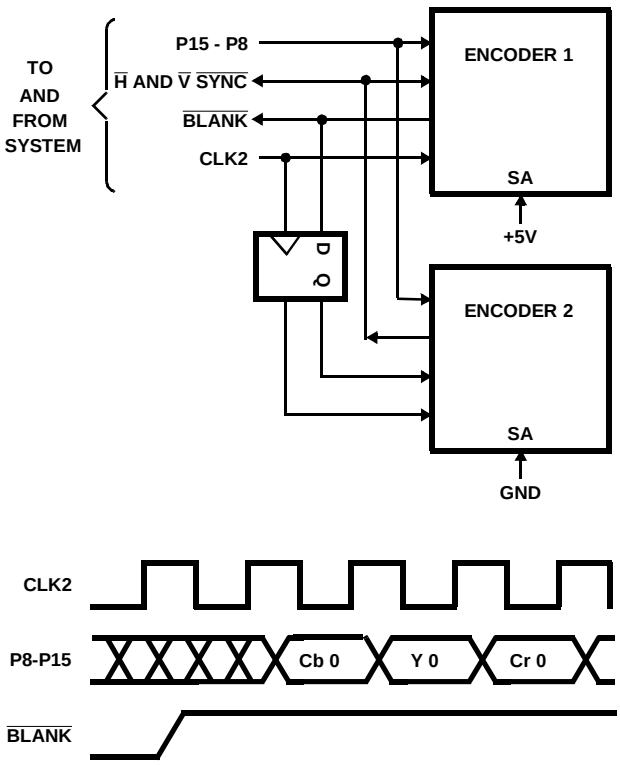

FIGURE 2. MIXED MASTER MODE CONNECTIONS AND WAVE FORMS FOR DELAYED DATA OUT

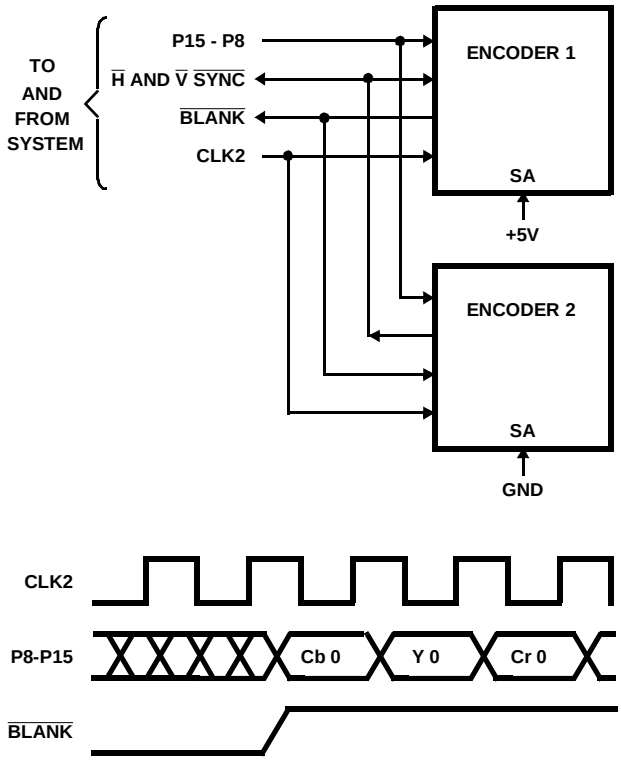

FIGURE 3. MIXED MASTER MODE CONNECTIONS AND WAVE FORMS FOR FAST DATA OUT

Since the video occurs at the same time while the syncs do not, the image from the first encoder will shift to the left. The shift is about 4 pixels wide.

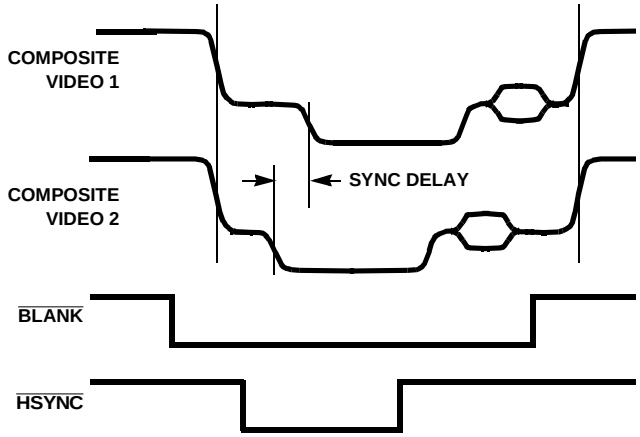

FIGURE 4. MIXED MODE VIDEO TIMING

The output timing may be aligned by delaying the H sync from the second encoder to the first. The delay required is one line time less 0.34µs. This large delay may be implemented using a pixel counter. The logic is simple since the pulse width of the H sync input to the encoder is not critical as long as it is at least two clocks wide. An example implementation is shown in Figure 5.

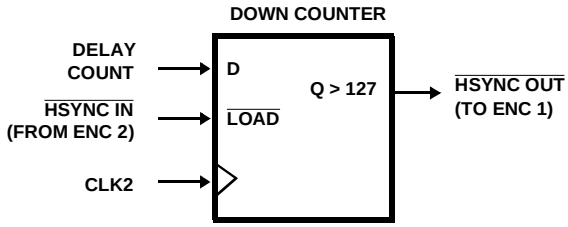

FIGURE 5. H SYNC DELAY LOGIC

The counter shown in Figure 5 is an 11 bit down counter with load. When the input H sync is asserted (low) then the counter loads the delay count needed (NTSC or PAL format and square or rectangular pixels). When H sync goes high again, the counter counts down each clock. When the counter value is greater than 127, the output H sync is high from the simple logical OR of the four MSBs of the counter. When the count does reach 127, the output H sync will be asserted. Before the count reaches zero, the next input H sync will occur and the cycle repeats. If the count does reach zero, it may roll over and continue down counting.

Validation

The mixed master modes have been demonstrated using the HMPVidEval/ISA PCI add in card with an HMP81xxEval1 daughter card. The register delay shown in Figure 2 was fly-wired in to the system using an ACT74 register. The H sync delay circuit has not been built or tested.

Dual Master Mode

Another method for connecting multiple encoders is dual master mode. In this mode, each encoder outputs its own sync and blank signals. The encoders are synchronized using parallel writes over the I^2C bus. The connections required for dual master mode are shown in Figure 6.

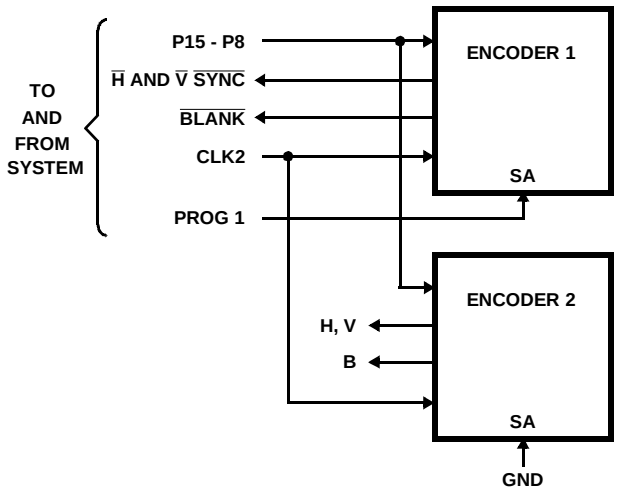

FIGURE 6. DUAL MASTER MODE CONNECTIONS

Programming Sequence

Dual master mode requires a special programming sequence in order to guarantee that the encoders are synchronized and that both sets of syncs and blank signals are the same. First, the software reset bit must be set in both encoders. Next, any programming that is common to both encoders must be done. Finally, the unique programming for each encoder may be sent.

For the software reset cycle and the common programming, the address select input must be the same for both encoders. Having multiple encoders use the same slave address does not cause any problems. Both encoders see the same I^2C inputs so they generate the same I^2C responses.

In order to program unique video outputs for each encoder, an additional signal to change one of the encoder's I^2C slave addresses is required. The slave address select input of one (and only one) of the encoders must toggle between the common and unique programming steps, while the I^2C bus is idle. The extra signal is named PROG1 in Figure 6.

I^2C Bus Synchronization

Using dual master mode also requires that the I^2C SDATA and SCLK signals be synchronous with respect to the encoders' CLK2 input. The SDATA and SCLK signals must meet setup and hold times at the rising edge of CLK2. If the I^2C controller is implemented in logic under the designer's control (CPLD, FPGA, ASIC, and/or microprocessor), then the circuit shown in Figure 7 may be used to synchronize the I^2C signals.

The controller shown in Figure 7 is a simple one which does not meet all of the requirements of the I^2C bus. However, it is sufficient for the Intersil encoders. The circuit shown assumes that

there are no other devices on the bus which may be bus masters. It also assumes that all devices on the bus are faster than the controller and will not hold SCLK low to extend bus cycles. The circuit also requires that WRITE EN only change when SDATA OUT is high and that WRITE EN be deasserted for the data acknowledge cycles from the slave device.

If the assumptions made for the circuits of Figure 7 are not met, then the alternate circuit shown in Figure 8 may be used for SDATA and/or SCLK. The circuit is more true to the I^2C specification. However, it may not be suitable if the external pull up resistor and/or net capacitance is large. In this case, the rise time of the signal will be too long and the setup and hold time with respect to CLK2 at the encoder may not be satisfied.

If the system's I^2C controller is not accessible and under the designer's control, then the circuit shown in Figure 9 may be used to synchronize the bus signals to the encoder CLK2 signal outside the controller. The drawback of this circuit is that it precludes reading values from the encoder. Some I^2C controllers may report errors if they do not read the bus acknowledge cycle from the target device. The circuit is similar to the one shown in Figure 8 and its rise time must be considered too.

Validation

The dual master mode has been demonstrated using the HMPVidEval/ISA PC add in card with an HMP81xxEval1 daughter card. Both boards provide a removable shunt to set the slave address select. One of the shunts was removed by hand at the correct time in the programming sequence. The I^2C controller on the VidEval board is implemented in an Actel FPGA and uses the SCLK circuit shown in Figure 7 with the SDATA circuit from Figure 8. The other circuits have not been built or tested.

Summary

This Application Note has shown three methods which may be used to connect multiple Intersil encoders in the same system. Slave mode is the most straight forward but requires a timing master elsewhere in the system. Mixed master mode is also straight forward but does not generate perfect, time aligned video without a delay counter. Dual master mode provides aligned video but requires extra programming hardware and software.

The connection methods shown in this Application Note were tested using Intersil designed evaluation boards. Additional information about the evaluation boards is available from the Intersil Corporation web site. Intersil evaluation boards may be purchased by contacting a Intersil sales office.

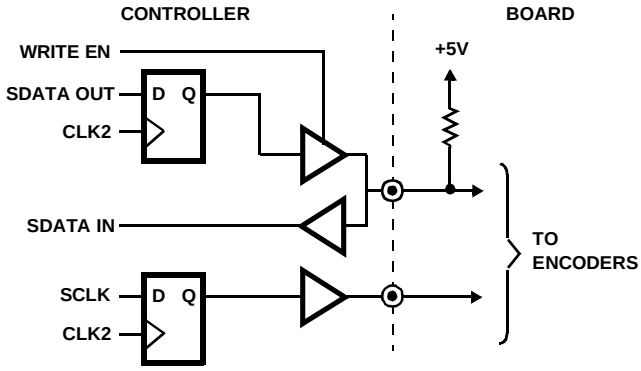

FIGURE 7. SYNCHRONOUS I^2C CONTROLLER

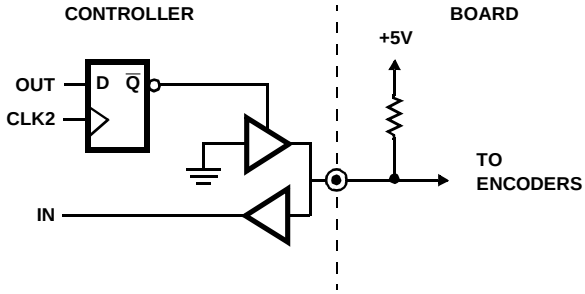

FIGURE 8. ALTERNATE SYNCHRONIZATION CIRCUIT FOR SDATA AND/OR SCLK

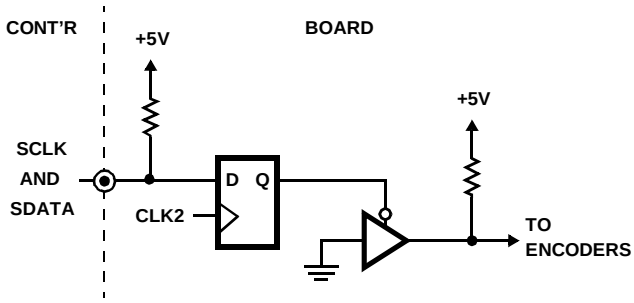

FIGURE 9. EXTERNAL WRITE ONLY I^2C SYNCHRONIZATION CIRCUIT FOR SDATA AND SCLK

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